

IN THE CLAIMS

Please amend the claims as follows:

Claim 1 (Canceled).

Claim 2 (Currently Amended): A processor system, comprising:

a first program storage which stores a first program;

a second program storage which stores a second program;

a program counter which outputs execution addresses of said first and second programs;

a first address storage which stores a first address in said first program;

a second address storage which stores a second address in said second program;

a comparator which compares whether or not said program counter coincides with said first address;

an address changing unit which changes said program counter to said second address, when it is determined to have coincided by said comparator;

a data bus which updates said first address stored in said first address storage and said second address stored in said second address storage; and

an instruction decoder which provides a result of decoding instructions read out from said first and second program storages to said data bus,

wherein said first address stored in said first address storage and said second address stored in said second address storage are updated based on ~~output~~ the result of said instruction decoder.

Claim 3 (Original): The processor system according to claim 2, wherein said first program includes:

a plurality of instructions which store a plurality of first addresses in said first address storage; and

a plurality of instructions which store a plurality of second addresses in said second address storage,

wherein said first address storage stores a plurality of first addresses in sequence, in accordance with said first program at timing different from each other; and

said second address storage stores a plurality of second addresses in sequence, in accordance with said first program at timing different from each other.

Claims 4-8 (Canceled).

Claim 9 (Currently Amended): A processor, comprising:

a program counter which outputs execution addresses of a first program stored in a first program storage and a second program stored in a second program storage;

a comparator which determines whether or not said program counter coincides with a first address in said first program stored in said first address storage;

an address changing unit which changes said program counter to a second address in said second program stored in said second address storage, when it is determined to have coincided by said comparator;

a data bus which updates said first address stored in said first address storage and said second address stored in said second address storage; and

an instruction decoder which supplies a result of decoding instructions read out from said first and second program to said data bus,

wherein said first address stored in said first address storage and said second address stored in said second address storage are updated based on the ~~output~~ result of said instruction decoder.

Claim 10 (Original): The processor according to claim 9, wherein said first program includes:

a plurality of instructions which store a plurality of first addresses in said first address storage; and

a plurality of instructions which store a plurality of second addresses in said second address storage,

the processor according to claim 9, further comprising:

a first address storing controller which performs control for storing in sequence a plurality of first addresses in said first address storage at timing different from each other, in accordance with said first program; and

a second address storing controller which performs control for storing in sequence a plurality of second addresses in said second address storage at timing different from each other, in accordance with said first program.

Claims 11-15 (Canceled).

Claim 16 (Currently Amended): An arithmetic processing method, comprising:

outputting from a program counter execution addresses of a first program stored in a first program storage and a second program stored in a second program storage;

determining whether or not said program counter coincides with a first address in said first program stored in said first address storage;

changing said program counter into a second address in said second program stored in said second address storage, when it is determined to have coincided; and

supplying a result of decoding instructions read out from said first and second program storages to said data bus,

wherein said first address stored in said first address storage and said second address stored in said second address storage are updated based on the ~~output~~ result of said ~~instruction decoder~~ supplying.

Claim 17 (Original): The arithmetic processing method according to claim 16, wherein said first program includes:

a plurality of instructions which store a plurality of first addresses in said first address storage; and

a plurality of instructions which store a plurality of second addresses in said second address storage,

and further comprising:

performing control for storing in sequence a plurality of first addresses in said first address storage at timing different from each other, in accordance with said first program; and

performing control for storing in sequence a plurality of second addresses in said second address storage at timing different from each other, in accordance with said first program.

Claims 18-20 (Canceled).